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KANG, S

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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-55 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-55 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

15. The drawings are objected to because Figures 1-8 are not designated by a legend such as "Prior Art". The legend is necessary in order to clarify what applicant's invention is. MPEP § 608.02(g). Correction is required.

16. Claims 3 and 13 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, ln3-"judging means for judging" is vague. Examiner suggest "judging" be replaced by "determining" for clarity; ln7,13,19-"a direction" is vague and indefinite.

Examiner suggest "the" be replaced by "said" in order to clearly identify claimed elements. For example, in claim 13, ln16 and ln19-"an overflow" should be "said overflow". ln15-"a user's direction" is vague and indefinite.

17. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

18. Claims 1-36 and 44-55 are rejected under 35 U.S.C. § 103 as being unpatentable over Harman in view of Sebesta.

As for claim 1, Harman shows MC68000 processor which has an addressing mode where memory, register and immediate values are used to access data and the addresses are extended to specification of the instruction like absolute short and long addressing (pg.145-146). Harman also shows extending data to certain data width depending on the instruction, from byte to word or long word before the data is used in operation (pg. 150). Thus, the processor can distinguish when the operands are used as a data or as an address depending on the opcodes and addressing modes. But, Harman does not explicitly shows that address and data width is held in parameter holding means to be used during translation. However, Sebesta shows concept of compilation and interpretation (pg.17-22).

The compiler goes through several analyzing steps like syntax, intermediate code generator, and code generator to convert the source program into target code. Thus, it would have been obvious to a one of ordinary skill in the art at the time of the invention in light of Harman and Sebesta to store the address and data width information so that compiler knows how wide to expend the data or an address. The reason for bit expansion is so that new processors that works with wider word (64 bits) can be compatible with older processors. Also, it makes the programmers job easier by not having to specifically give full bit width every time they are instructing to perform calculation. For example programmer does not have to always type: ADD Hex.0001,R1 for 16 bit architecture, instead ADD Hex.1,R1 would do the same.

For claims 2, 4 and 7, Harman and Sebesta show everything listed above. Furthermore, it is well known in the art to have data word size of 16 bits and address length of 32 bits. However, not all 32 bits of address is used to address a data. For example, MC68000 uses 32 bit program counter but only 24 bits are used to address an instruction. Therefore, it would have been obvious to a one of ordinary skill in the art at the time of the invention to set address range from 17 to 31 bits to uniquely identify entire memory space local and external.

For claim 3, Harman shows MC68000 processor that has an instruction that uses memory, register and immediate value as an

operands to perform specific opcodes (pg 94). Thus, the processor has the means to process instruction with variety of addressing modes and data sizes. Also, data and address expansion with data and address size being different is well known in the art and depending on particular instruction, the memory, register and immediate value can be used as data or as an address (MC68000, pg 110-111). Furthermore, it is well known in the art that a compiler which runs on MC68000 processor will expend data and addresses to its full bit width when generating object code that machine executes.

For claim 5, Harman and Sebesta show everything listed above and also address expansion is well known in the art, thus if the addressing takes 24 bits to address a data then any address supplied to the processor is expended to the full 24 bits. Therefore, if the processor architecture utilizes 16 bit addresses then that processor will expend every addresses to 16 bits before that address is accessed.

For claim 13, Harman shows detection of an overflow and notifying of the overflow to the user for correction (pg. 197). It is well known in the art that overflow occurs when the result of an operation exceeds the set aside data width for that data type result. But, Harman does not explicitly shows that overflow compensate instructions are generated as the possibility of overflow is detected. However, it would have been obvious to a one

of ordinary skill in the art at the time of the invention to supply user specified overflow compensation to make the compiler more automatic. Therefore, the occurrence of an overflow is reduced, hence making the processor execute program faster. The rest of the claim is rejected based on same rationale as set forth in claim 1.

For claim 15, 64-bit architecture is well known in the art. Thus, same principles of 16 and 32 bit architecture applies to the 64-bit architecture. Therefore, it would have been obvious for 64-bit architecture to have address width less than or equal to 64 and more than or equal to 33 bits like MC68000, which is 32 bit architecture but uses 24 addressing bits, and have data size of 32 bits.

For claim 16, as listed above and in claim 13, detecting possible overflow by checking operands signs are well known in the art along with zero and sign extension to expand bits.

For claim 27, as shown in above claims 20, 23 and 24, Harman and Sebesta show processor and compiler. The compiler runs on processor and it converts source code into target code. Thus, claim 27 as a hole is a combination of claim 20, 23 and 24 and hence it is rejected based on those same rationale because compiler and processor which is well known in the art performs functions claimed in claim 20, 23 and 24.

For claim 28, a processor consisting of memory, program counter, instruction fetch and executing means where address is

calculated separately from the data is well known in the art to speed up the processing.

For claim 29, a processor containing address and data registers are well known in the art. See Harman pg. 85.

For claim 30, MC 68000 is a single chip processor that utilizes 24 bit addressing and can access word size data (16 bits) and can address over 64Kbyte memory space (pg. 30).

For claim 31, Harman and Sebesta showed as listed above, a way to detect possible overflow instruction. But Harman does not explicitly show to expend the data field to 24 bits. However, it would have been obvious to a one of ordinary skill in the art at the time of the invention to solve the overflow problem by using the compiler to insert compensating instruction to expend the data width to catch the overflow. Since most processors are byte accessible, it would have been obvious to expend from 16 to 24 bit-width to solve the overflow problem without wasting too much memory space.

For claim 32, extending sign bit and zero bits to fill the data or address width is well known in the art.

For claims 44 and 47, operating, instruction control and instruction decoding means are well known in the art to perform calculation and decoding whether the data belongs in data or address register. Thus, the scope of the claim has not changed because the feature claimed is part of the processor. Therefore,

claim 44 is rejected based on same rationale as set forth in claim 29 and 31.

For claim 49, Harman shows MC68000 instruction which has address mode to load immediate value into the data or address register and to add or subtract immediate value from/to data or address registers.

For claims 51-52, Harman shows MC68000 processor, which has plurality of data and address registers, decodes the instruction and extends zero or sign of the operands to the specified data width and that extended values are used in the calculation.

For claim 54, Harman shows that condition fields, which is plurality of flag fields, are used in operation to determine the condition for branch (pg. 175). Therefore, the rest of the claims are rejected based on same rationale as set forth in claim 28, 32, 13 and 37 because claimed invention as a whole is obvious from the disclosure by the Harman.

Claims 6-13 are rejected based on same rationale as set forth in claims 1-5. Claim 6, syntax analyzing and generating variable table from the parsing for the compiler is well known in the art. The task of compiler is well known in the art. The compiler analyzes the syntax, build the table and applies target architecture parameters to translate source code into target code. Thus, expending on the features of compiler does not change the scope of the claim. Therefore, claim 6 is rejected based on same

rationale as set forth in claim 1. Claim 11 is same as claim 6 and 8; Claim 12 is same as claim 10; Claims 14 and 21 are same as claim 2; Claims 17, 24 and 18, 25 are same as claims 3 and 4; Claims 19 and 26 are same as claim 15; Claim 20 is same as claims 6 and 13; Claim 22 is same as claim 15; Claim 23 is same as claim 16; Claims 33-36 are same as claims 29-32; Claims 45 and 46 are same as claims 29 and 30; Claim 48 is same as claim 45; Claims 50, 53 and 55 are same as claim 46;

19. Claims 37-43 are rejected under 35 U.S.C. § 103 as being unpatentable over Harman and Sebesta as applied to claim 29 above, and further in view of Applicant's admission.

As for claim 37, Harman and Sebesta shows everything listed above but do not explicitly show external-access-width control and external-access executing means to transfer data between the processor and external memory. However, Applicant admits (pg. 4&5) that external storage and external-access executing unit for inputting and outputting data of designated bit-width with the external storage memory unit 13. Therefore, it would have been obvious to a one of ordinary skill in the art at the time of the invention to add external accessing feature to the processor to access external memory. Also, it is well known in the art for processor to access the external memory and for the processor to

specify the bit-width information since communication takes place in 8 or 16 bits.

For claims 39 and 40, Harman shows that byte, word or long word of a register can be written/read to/from the memory. But, he does not explicitly shows that registers are 24-bit and that transmission width is 8-bit wide. However, byte and word wide data transmission are well known in the art. Thus, it would have been obvious to a one of ordinary skill to transmit 24-bit (3 byte) in three transmission and 16-bit (2 byte) in two byte transmission from the processor to the external memory and two and one word transmission for 16-bit transmission line.

For claim 41, it is well known in the art for the data transmission to buffer transmitting and receiving data and to split long word into transmission width. Thus, 64-bit word transmission in 8-bit transmission line would break 64-bit into eight byte for transmission. The counter utilized in data transmission is well known to, for example, count off eight byte transmitted above.

The following claims are rejected based on the rationale as set forth in above claims. Claim 38 is same as claim 27; For claim 42, the same principle of 24 bit applies, therefore it is same as claim 40; Claim 43 is same as claim 41;

20. Other references of general interests are listed below:

A. Baum et al. (U.S.PN:4739471) Method and means for moving bytes in a reduced instruction set computer.

B. Fong (U.S.PN:4447879) Improved apparatus for representing the size of an element in a compound data item and deriving addresses and lengths using the element size.

C. Hopkins et al. (U.S.PN:4763255) Method for generating short form instructions in an optimizing compiler.

D. Ikeya (U.S.PN:4602330) Data processor.

E. Benson (U.S.PN:5307492) Mapping assembly language argument list references in translating code for different machine architectures.

F. Hennessy et al., Computer Architecture A Quantitative Approach, 1990.

21. Any inquiry concerning this communication should be directed to Sang Yong Kang at telephone number (703) 305-9659.

22. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

DAVID Y. ENG
PRIMARY EXAMINER
ART UNIT 232